

<b>Notice of References Cited</b>	Application/Control No. 10/623,083	Applicant(s)/Patent Under Reexamination CHONG ET AL.	
	Examiner Pierre-Michel Bataille	Art Unit 2186	Page 1 of 1

#### U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,198,686	03-2001	Takita et al.	365/230.06
*	B	US-5,243,703	09-1993	Farmwald et al.	713/400
	C	US-			
	D	US-			
	E	US-			
	F	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

#### FOREIGN PATENT DOCUMENTS

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#### NON-PATENT DOCUMENTS

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*	U	Yasunobu Nakase, et al., Source-Synchronization and Timing Vernier Techniques for 1.2-GB/s SLDRAM Interface, IEEE Journal of Solid-State Circuits, vol. 34, No. 4, pp. 494-501, Apr. 1999.
*	V	Song et al., "NRZ Timing Recovery Technique for Band-Limited Channels," IEEE Journal of Solid-State Circuits, vol. 32, No. 4, pp. 514-520, Apr. 1997.
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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